SIGNAL TRANSMISSION SYSTEM WITH PROGRAMMABLE VOLTAGE REFERENCE

TECHNICAL FIELD

The present invention relates in general to circuits for transmitting digital signals between integrated circuits on circuit lines treated as transmission lines.

BACKGROUND INFORMATION

Computer systems typically have the integrated circuits (ICs) interconnected on a motherboard. These ICs send signals between various circuit functions using drivers and receivers. On-chip circuits use drivers and receivers configured for the on-chip transmission lines which are typically very short but highly resistive and lossy. Off-chip drivers are used for signals transmitted between ICs. As off-chip communication speeds have increased, the lines interconnecting the ICs should be treated as transmission lines when their lengths are long relative to the fundamental wavelengths of the signals they transmit. Off-chip transmission lines are typically low-loss with characteristic impedances typically between 50 and 70 ohms.

Off-chip drivers that have signal swings extending to the power supply rails require high currents relative to the currents for on-chip driver circuits. As off-chip driver speeds have increased so has the number of bits for the data buses used in off-chip communication. Most logic in the various ICs making up a computer system are synchronous, wherein a system clock is used to time when data is transmitted or applied to one end of a transmission line and when it is sampled by the receiver at the other end of the transmission line.

Various types of noise may result from off-chip driving including simultaneous switching noise, electric and magnetic field coupling between signal transmission lines,

etc. Likewise, the power supply noise resulting from large current spikes during simultaneous switching in an IC transmitting signals may be different from the power supply noise present at an IC receiving the signals. As system clocking speeds have increased, the power supply voltages have been decreased to manage power. The higher speed operation along with lower power supply voltages may lead to decreased noise margins. Some of the noise experienced in off-chip communication may be common mode where the noise appears simultaneously on both the voltage and ground lines (planes) of the motherboard. To improve the noise rejection when receiving off-chip signals, differential receivers are often used where the receivers are biased at a reference level (e.g., one half the power supply voltage).

It is also advantageous to terminate the transmission lines interconnecting ICs in the characteristic impedance of the transmission line. While the transmission line may be series or source terminated, far end termination often provides the best overall performance at the expense of power dissipation especially when the transmission line network has multi-drop nets (e.g., a particular bit is coupled to more than one IC). All the above factors create a signal transmission environment which is difficult to optimize so as to ensure the best possible noise margins.

There is, therefore, a need for signal transmission circuitry and a method for optimizing the noise margins in high speed digital signal transmission and reception.

SUMMARY OF THE INVENTION

Embodiments of the present invention disclose a signal transmission system and method for communication between integrated circuits (ICs) where the clock rates are at a frequency where the signal lines must be considered as transmission lines. The signal transmission system uses data line drivers that are each far-end terminated in a termination network which is coupled to one input of a differential receiver; the second input of the differential receiver is coupled to a reference network. The termination network generates a termination voltage by dividing the receiver power supply voltage in a programmable voltage divider network that allows the reference voltage to be varied up and down while maintaining a constant termination impedance. The data is clocked at the driver by a clock signal whose output levels are a function of the driver power supply voltage. Likewise, the data signals have output levels that are functions of the driver power supply voltage. At the same clock time that the data signals are transmitted, a clock and an inverted clock are transmitted using line drivers like those for the data signals. The clock signals are each terminated in a termination network like the data lines. In addition, each clock signal is coupled through a resistor/capacitor filter network to an output node generating the reference voltage. Since one of the clock signals is always at a logic one, representative of the driver power supply, the output node of the clock termination network has a variation corresponding to the driver power supply voltage at the time of signal transmission. The data termination networks have programmable resistor dividers that allow the termination voltage to be varied under system control to optimize noise margins or to test the signal transmission network. The clock termination voltage has filtered variations of the driver and receiver power supply voltages coupled to it to allow the threshold level of the receivers to track changes in the driver power supply voltages to further optimize noise margins.

The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be described hereinafter which form the subject of the claims of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a block diagram of a signal transmission system according to embodiments of the present invention;

FIG. 2 is a detailed circuit diagram of an embodiment of the present invention showing data and clock lines terminated at receivers;

FIG. 3 is a detailed circuit diagram of a programmable terminator according to embodiments of the present invention;

FIG. 4 is a table illustrating programming of the terminator of FIG. 3; and

FIG. 5 is a block diagram of a data processing system suitable to practice embodiments of the present invention.

DETAILED DESCRIPTION

In the following description, numerous specific details are set forth to provide a thorough understanding of the present invention. However, it will be obvious to those skilled in the art that the present invention may be practiced without such specific details. In other instances, well-known circuits have been shown in block diagram form in order not to obscure the present invention in unnecessary detail. For the most part, details concerning timing considerations and the like have been omitted in as much as such details are not necessary to obtain a complete understanding of the present invention and are within the skills of persons of ordinary skill in the relevant art.

Refer now to the drawings wherein depicted elements are not necessarily shown to scale and wherein like or similar elements are designated by the same reference numeral through the several views. In the following detailed descriptions, a logic zero is a low or zero voltage and a logic one is a high or a plus supply voltage to simplify explanation of embodiments of the present invention.

FIG. 1 is a block diagram of a signal transmission system according to embodiments of the present invention. A data signal 101 is coupled to driver (DR) 103 which is "clocked" by clock (CLK) signal 116. DR 103 is powered by power supply (PS) 102 and generates a data output (DO) signal 104 in response to clock edges of CLK signal 116. DO signal 104 is transmitted by transmission line (TL) 105 to receiver (REC) 112 which is powered by PS 107 which has a return ground 127. PS 102 and PS107 may be the same potential but are differentiated because they may be remote from each other and may have different noise conditions. All the ground returns of PS 102 and PS 107 may not be shown or labeled in FIG. 1 to simplify the drawing. REC 112 generates receiver output 111 in response to the difference in the voltages received on it inputs 109 and 110. In a synchronous system, REC 112 is "sampled" by edges of a clock synchronous with CLK 116. Termination network (TN) 108 is used to match the

impedance of the receiver to the characteristic impedance of TL 105. TN 108 generates a termination voltage (VT) 109 and has a termination source impedance (ZT). TN 108 is programmed by program signals 106 to vary VT 109 while keeping ZT at a fixed value. ZT is not shown in FIG. 1 but is internal to the termination network 108. Clock driver (CDR) 119 receives CLK signal 116 and generates a clock output (CLK_Out) signal 117 and a complement CLK_Out signal 118. CLK_Out 117 is transmitted on TL 114 and received at output 120 which is coupled to reference network (RN) 113. CLK_Out 118 is transmitted on TL 115 and received at output 121 which is also coupled to reference network (RN) 113. RN 113 comprises TN 123 for TL 114 and TN 124 for TL 115. The outputs of TN 123 and 124 are coupled to a filter network (FN) 125 which generates reference output 110. RN 113 is programmed with program signals 122. RN 113 generates an output 110 in response to the received CLK_Out 117 and 118 . Output 110 is coupled to REC 112 and generates a modified threshold voltage for REC 112.

A repetitive data pattern may be transmitted on a TL 105. When a repetitive data pattern is transmitted and received, successive transitions between a logic one and a logic zero, after reception, may not happen at precisely the same time even though they may have been transmitted at the same time. This is due to the uncertainties in the transmission and detection during reception of the transmitted data in exemplary REC 112. If one views a transition of a repetitive data pattern on an oscilloscope, an "eye" pattern would be apparent. This occurs as a particular observed transition in the repetitive data pattern varies around the ideal timing due to uncertainties. The eye pattern results as a larger number of transitions occur on either side of an ideal transition timing leaving an open area in the display.

Using a repetitive data pattern, termination network 108 may be programmed with program signals 106 to vary VT 109 while keeping the termination impedance ZT constant. Per bit error registers may be used in a system that employs signal transmission

according to embodiments of the present invention to log failures that occur on received signals from output 111. Stress tests may be exercised to determine failure margins by varying exemplary voltage VT 109 while monitoring the error rate of the output of exemplary REC 112. Only one data line (e.g., DO 104) is shown in FIG. 1 to simplify the drawing. It is understood that embodiments of the present invention use multiple data lines with corresponding drivers, transmission lines, termination networks, program signals and receivers.

FIG. 2 is a circuit diagram of multiple data signals (D 206- D 208) with corresponding transmission lines (TL-211- TL 213) and receivers (REC 223-REC 225), respectively. Nodes 230-232 are terminated in voltage divider termination networks TN 216-TN 218. A termination network (e.g., TN 216) is designed to have terminator voltage (V 230) determined by PS 107 and the divider ratio of resistors 228 and 229. While the resistors in each of the dividers 216-220 are shown fixed resistors, dividers 216-220 may receive program inputs which allow characteristics of the dividers to be varied. The programming of dividers 216-220 is not shown in FIG. 2 for simplicity, but a divider may be like a programmable divider 108 as shown in FIG. 3.

A differential receiver (e.g., REC 223) receives a reference voltage VREF 226 and generates an output in response to the difference in the voltages received on its inputs. Common mode noise (noise appearing of both the power supply 107 and ground 127 is reduced (rejected) by the differential characteristics of a differential receiver (e.g., REC 223). Clock driver DR 204 transmits CLK_Out 209 on TL 214 to TL output 233 which is terminated in TN 219. Likewise, the complement clock CLK_NOut 210 is transmitted on TL 215 to TL output 234 which is terminated in TN 220. TL output 233 is coupled to capacitor (C) 227 with resistor (R) 221 and TL output 234 is coupled to C 227 with R 222. C 227 operates to low pass filter the signals on TL output 233 and TL output 234 to modify VREF 226. C 227 may be configured as two capacitors of one-half

the value of C 227, one from VREF 226 to ground 127and one from VREF 226 to the power supply voltage 107. VREF 226 will be a composite of the direct current (DC) levels on node 233 and 234 as well as the filtered alternating current (AC) signals caused by the dynamics of CLK_Out 209 and CLK_NOut 210. Either CLK_Out 209 or CLK_NOut 210 is always at a logic one except for the times the two signals have concurrent signal transitions. R 221 and R 222 may be sized along with C 227 so that VREF 226 has a level that tracks the low frequency variations of PS 102 and PS 107. These low frequency variations may be caused by distribution losses, simultaneous switching noise, or other noise sources. If these variations appear on both the clock signals and the data signals, then the receivers (e.g., REC 223-REC 225) reduce the effects of the variations by their common mode rejection characteristics. Additionally, if TN 216-TN 220 are programmable, then the terminating voltages on nodes 230-232 may be modified to optimize signal detection and improve noise margins.

FIG. 3 is a circuit diagram of exemplary termination network TN 108 which is programmable with program signals 106 according to embodiments of the present invention. In one embodiment of the present invention, resistors R 325-R 344 all have the same value. R 325-R 329 and R 335-R 339 are grouped in one circuit corresponding to their common program signal (PRS) 301. If PRS 301 is a logic zero, then R 325-R 329 are coupled in parallel to node 109 and PS 107. Likewise if PRS 301 is a logic one, then R 335-R 339 are coupled in parallel to node 109 and ground 127. The resistors R 325-R 334 and R 335-R344 are selected in a group of five, one, and two groups of two. This allows the selection of all groups of resistors in pairs (5,5), (6,4), (4,6), (7,3), (3,7), (8,2), (2,8), (9,1), (1,9) (10,0) and (0,10). The fact that the resistors are the same value allows the parallel combination of the resistors as "seen" at node 109 to always be a constant resistance. For example, if each resistor R325-R344 is 500 ohms, then the circuit in FIG. 3 allows the voltage at node 109 to be varied from PS 107 to ground 127

in ten incremental steps. Likewise, the resistance as seen at node 109 is a constant 50 ohms, 500 ohms divided by 10. Ten is the number of resistors in each possible parallel grouping.

It may be desirable to make the terminating networks out of groups of like resistors to improve matching. For the above example ten parallel 500 ohm resistors are used for the upper and lower branches for TN 108. Other values of resistors may be used for other impedances by scaling the resistor values. If it is desired to use groups of like resistors to generate a number of N increments of the terminating voltage according to embodiments of the present invention, there is only one minimum number of M of program inputs 106 corresponding to each number N. For N=10 there are a minimum of four parallel networks with equivalent branch resistances of, 500 ohms, 250 ohms, 250 ohms and 100 ohms. If twelve increments of the terminating voltage are desired, while maintaining a terminating resistance of 50 ohms, then twelve 600 ohm resistors grouped in four parallel networks would be necessary with equivalent branch resistances of, 600 ohms, 300 ohms, 200 ohms and 100 ohms. Other increments may be used and still be withing the scope of the present invention.

In FIG. 4, table 401 shows the number of parallel resistors in columns 402 (for ten increments) in the "UP" circuit (circuit between node 109 and PS 107) and the "DOWN" circuit (circuit between node 109 and ground 127). The columns 403 in table 401 list the states of the program signals P1 301, P2 302, P3 303 and P4 304 used to generate the variable termination conditions on node 109. Columns 405, in table 402, list the resulting parallel resistances of the UP circuit and the DOWN circuit. The resulting terminator source resistance is shown in column 404.

FIG. 5 is a high level functional block diagram of a representative data processing system 500 suitable for practicing the principles of the present invention. Data processing system 500, includes a central processing system (CPU) 510 operating in

conjunction with a system bus 512. System bus 512 operates in accordance with a standard bus protocol, such that as the ISA protocol, compatible with CPU 510. CPU 510 operates in conjunction with electronically erasable programmable read-only memory (ROM) 516 and random access memory (RAM) 514. Among other things, ROM 516 supports storage the Basic Input Output System (BIOS) data.. RAM 514 includes, DRAM (Dynamic Random Access Memory) system memory and SRAM (Static Random Access Memory) external cache. I/O Adapter 518 allows for an interconnection between the devices on system bus 512 and external peripherals, such as mass storage devices (e.g., a hard drive, floppy drive or CD/ROM drive), or a printer 540. A peripheral device 520 is, for example, coupled to a peripheral control interface (PCI) bus, and I/O adapter 518 therefore may be a PCI bus bridge. User interface adapter 522 couples various user input devices, such as a keyboard 524, mouse 526, touch pad 532 or speaker 528 to the processing devices on bus 512. Display 538 which may be, for example, a cathode ray tube (CRT), liquid crystal display (LCD) or similar conventional display units. Display adapter 536 may include, among other things, a conventional display controller and frame buffer memory. Data processing system 500 may be selectively coupled to a computer or telecommunications network 541 through communications adapter 534. Communications adapter 534 may include, for example, a modem for connection to a telecom network and/or hardware and software for connecting to a computer network such as a local area network (LAN) or a wide area network (WAN). CPU 510 may comprise one or more processor ICs with one or more line drivers (e.g., DR 103) transmitting data (e.g., DATA 101) and clock signals (e.g., CLK_Out 117 and CLK_ONout 118) on motherboard transmission lines (e.g., TL 105, TL 114 and TL 115) to supporting ICs that have one or more corresponding differential receivers (e.g., REC 112), termination network (e.g., TN 108) and a reference network (e.g., RN113) while using embodiments of the present invention to optimize or test noise

margins. Likewise, CPU 510 and other components of data processing system 500 may transmit data and clock signals on motherboard transmission lines (e.g. TL 105, TL 114 and TL 115) to subsystems (e.g. RAM 514) which have one or more receivers (e.g., REC 112) coupled to termination networks(e.g, TN 108) according to embodiments of the present invention. CPU 510 may contain circuits for modifying a terminating voltage level (e.g., VT 109) of a termination network (e.g., TN 108) while maintaining a constant source impedance to set or test noise margin according to embodiments of the present invention.

The present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims.